

ABSTRACT OF THE DISCLOSURE

An apparatus and technique for monitoring clock in a data communication system is capable of conducting a more accurate monitoring on loss of clock for a synchronous signal, to measure stability between a bus synchronous signal and a clock for matching data transmission-receiving with a higher accuracy. The clock monitoring apparatus includes a first buffer block, a first counter block, a comparison block, a pulse generation block, a second counter block, and a second buffer block. If a clock provided from a system bus is abnormal, a different value from a normal value (namely reference value, e.g. 1024) is obtained at the first counter block. In this case, the comparison block outputs a value '1' to the pulse generation block, and the moment the pulse generation block receives the value '1', it generates a pulse, and the second counter block counts the number of pulses generated by the pulse generation block. Based on the number of pulses generated during a monitoring cycle, it is possible to detect how many times clock has been lost. When the monitoring result is stored in the second buffer block, a system control block (i.e. CPU) reads out the stored value and figures out the stability of clock of the system. Therefore, the present invention can be advantageously used for more accurately identifying the cause of data loss and measuring the stability of synchronous and clock signals in system, by checking or monitoring any occurrence of clock loss using the synchronous signal as a reference and providing this monitoring result to the CPU.